Analog Peak Detector and Derandomizer

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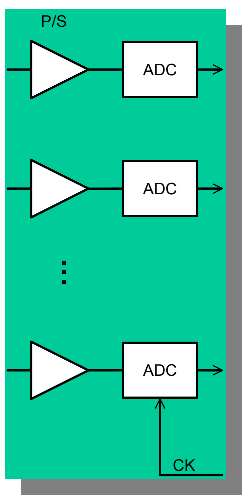
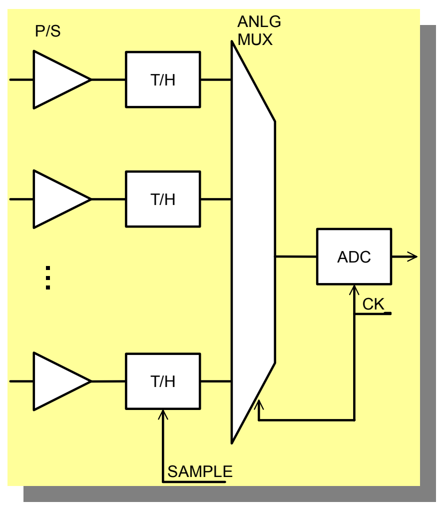
Multichannel Readout Alternatives

Direct digitization



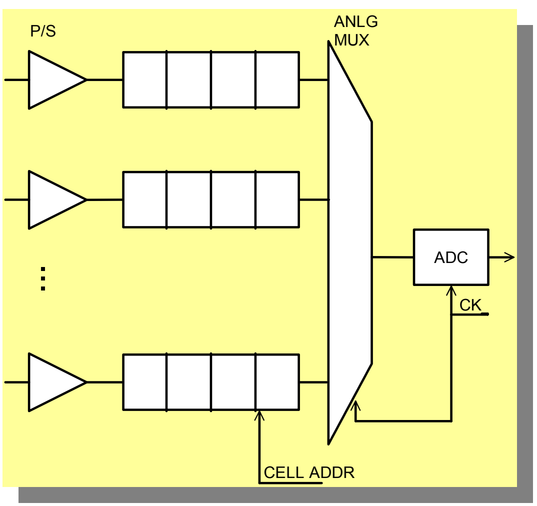
- most flexible
- requires many fast ADCs
- expensive, high power

Track-and-Hold + Analog Multiplex



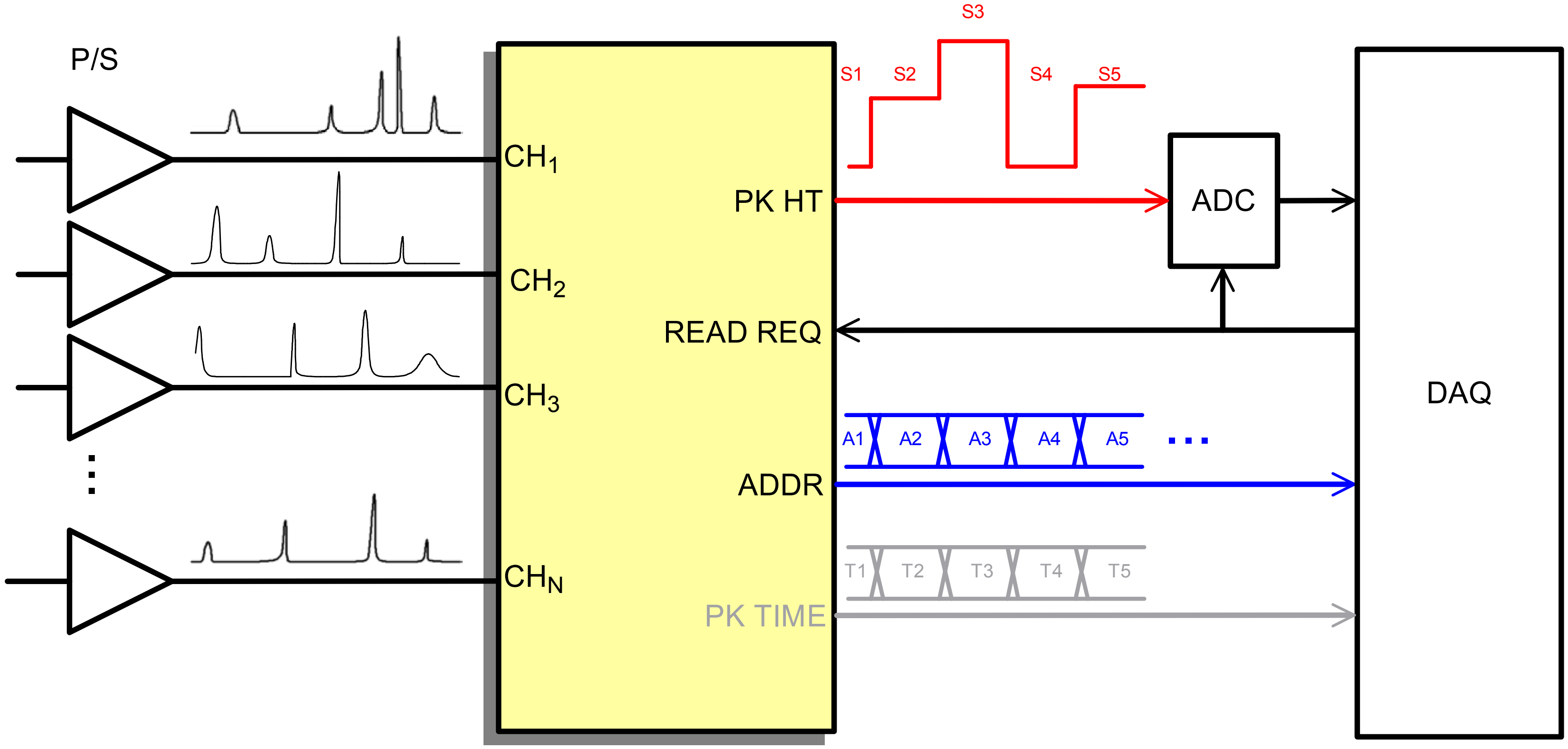
- requires trigger
- has deadtime
- timing uncertainty
- requires sparsification

Analog Memory + Analog Multiplex

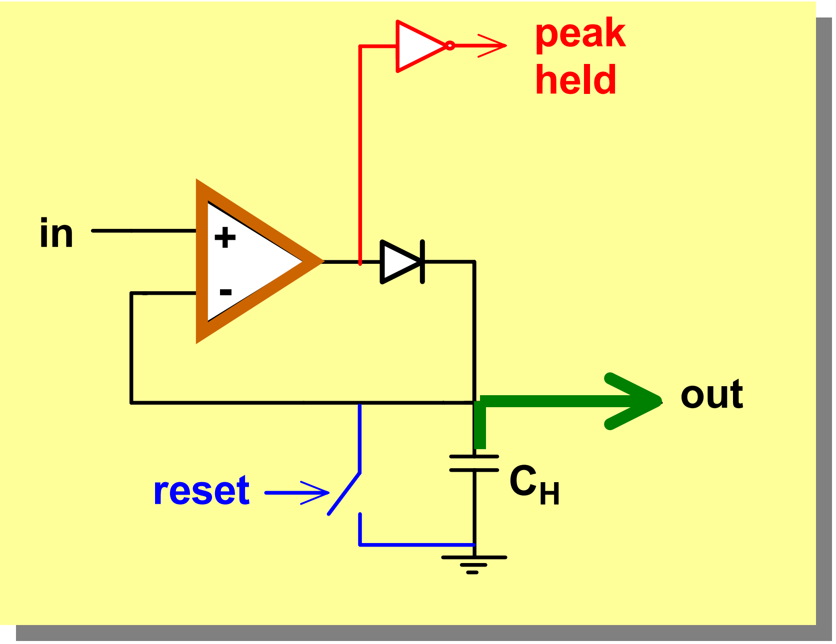


- requires trigger
- can be deadtimeless (complex control)
- requires sparsification

Ideal Self-triggered, Self-sparsifying, Deadtimeless Readout



Peak Detector (PD)



Advantages

- self-triggering
- self-sparsifying
- timing output

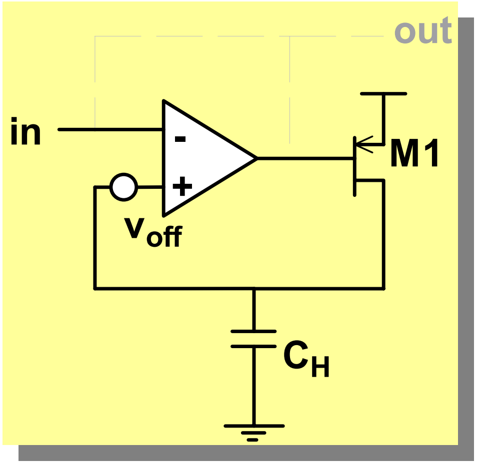
Drawbacks

- accuracy impaired by op-amp offsets, CMRR, slew rate
- poor drive capability
- deadtime until reset

Improved CMOS PD Using Two-Phase Configuration

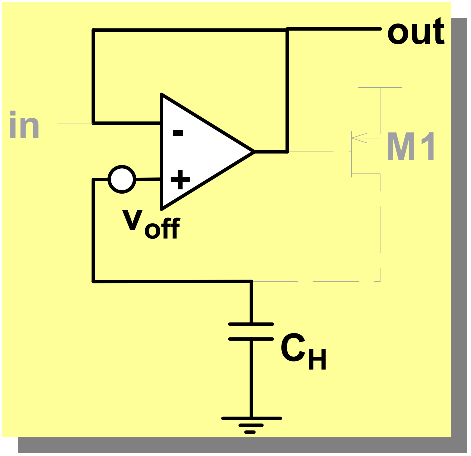
Write phase

- conventional peak detector
- M1: unidirectional current source
- voltage on C_H includes op-amp errors (offset, CMRR)



Read phase

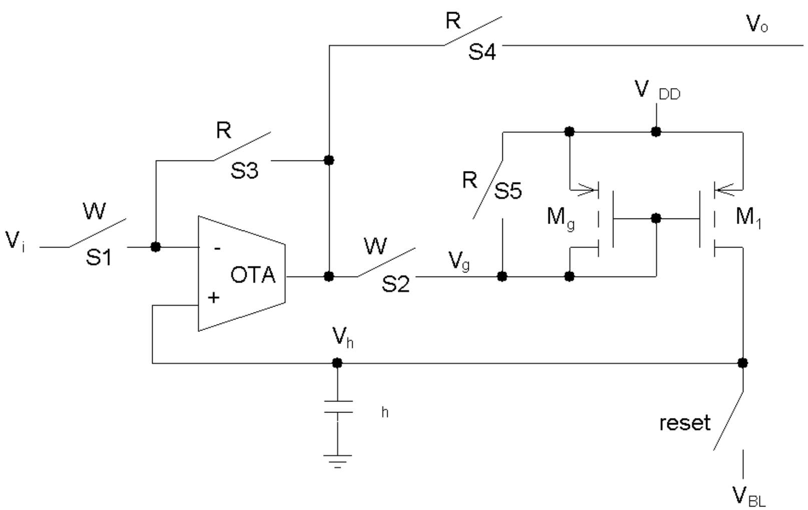
- same op-amp re-used as unity-gain buffer
- same CM voltage
- ***op-amp errors cancel***
- enables rail-to-rail sensing
- provides good drive capability



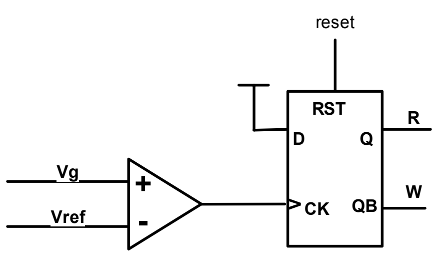
Two-Phase Peak Detector in 0.35 μm CMOS

SCHEMATIC

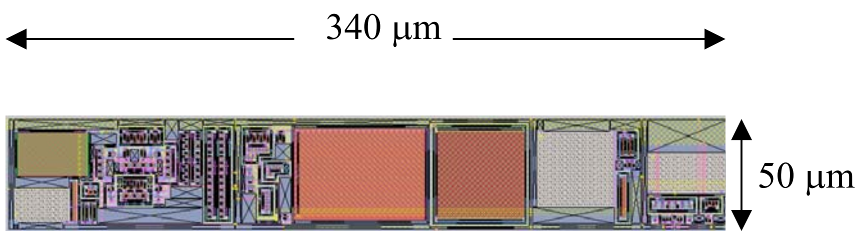
PD loop with switches

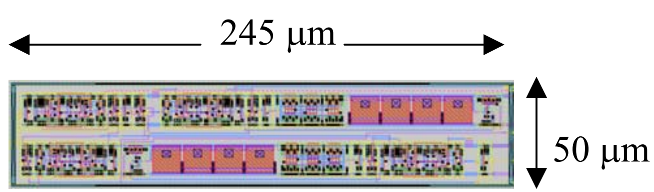


Switch control logic (*data driven*)



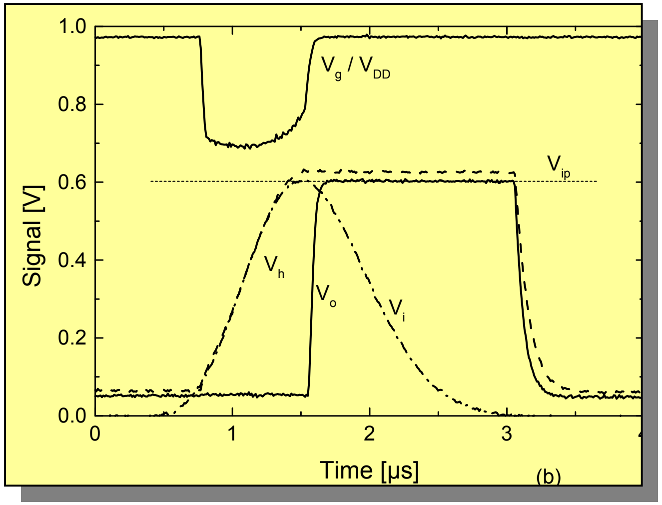
LAYOUT



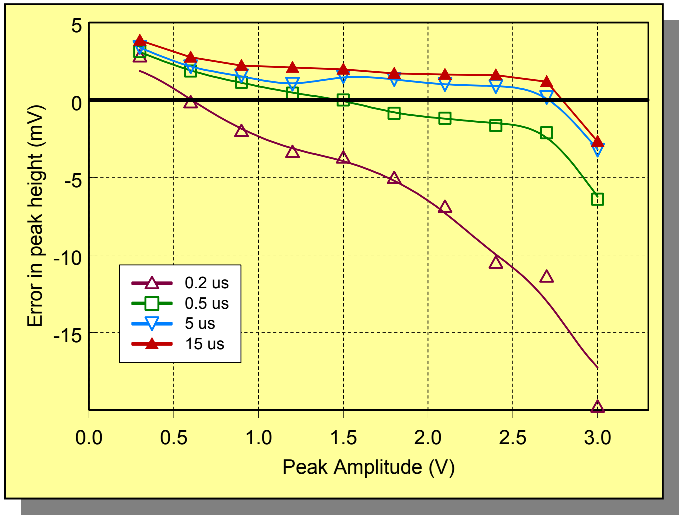


Two-Phase CMOS Peak Detector - Results

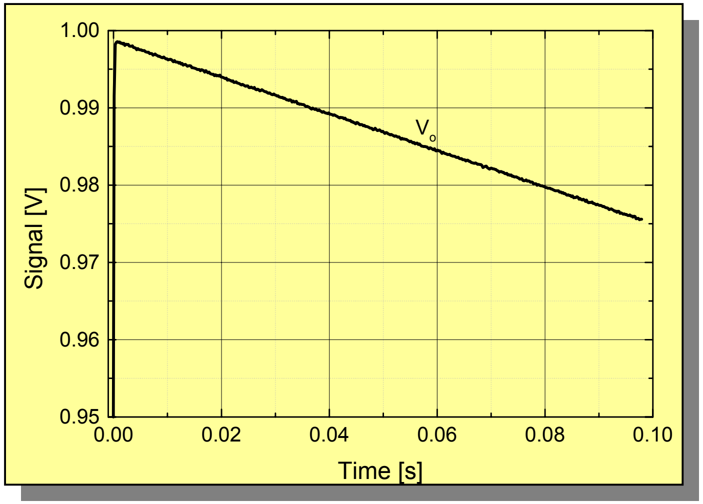
Waveforms



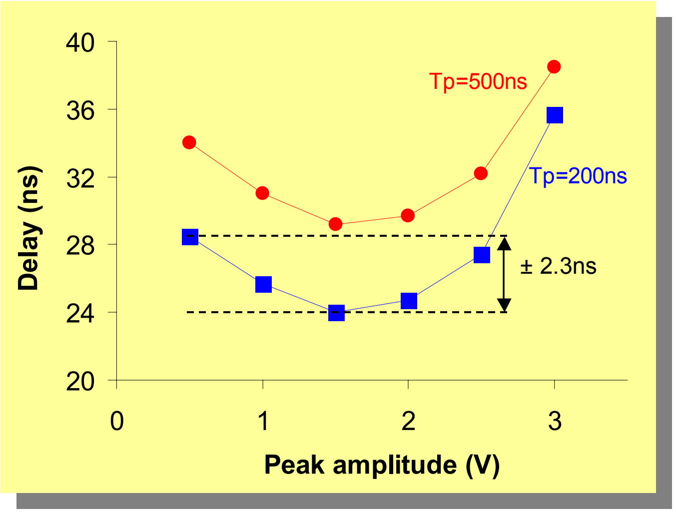
Absolute accuracy



Droop rate



Time walk



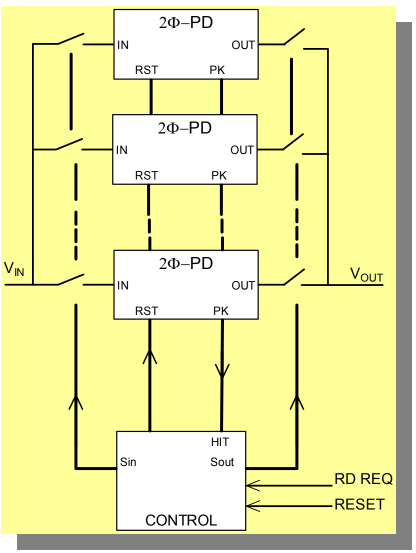
Two-Phase CMOS Peak Detector - Summary

- Self-triggering
- 2-phase operation eliminates op-amp errors
  - *High absolute accuracy independent of process, supply, temperature variation*
  - *Rail-to-rail input and output*
- Strong drive capability
- No switch charge injection into hold node
- Timing output

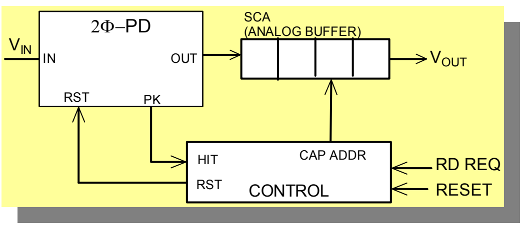
Parameter	***Value***
Technology	0.35 μm CMOS DP4M
Supply voltage	3.3 V
Input voltage range	0.3 – 3 V
Absolute accuracy	0.2 %, $t_p \geq$ 500ns 0.7%, t_p =200ns
Time walk	± 2.3 ns, V_{in} < 2.5 V ± 5 ns, V_{in} < 3 V
Droop rate	0.25 V/s
Power dissipation	3.5 mW
Cell area	0.03 mm^2

Peak Detector and Derandomizer

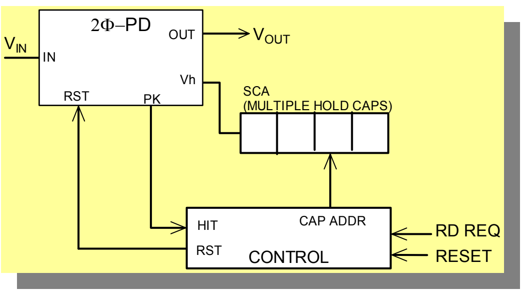
- Combine the peak detect and analog hold functions of the PD with additional analog storage and control logic to create a Peak Detector–Derandomizer (PDD).
- PDD behaves like a data driven, analog FIFO memory.
- Topologies:



A: Array of PD with ping-pong control



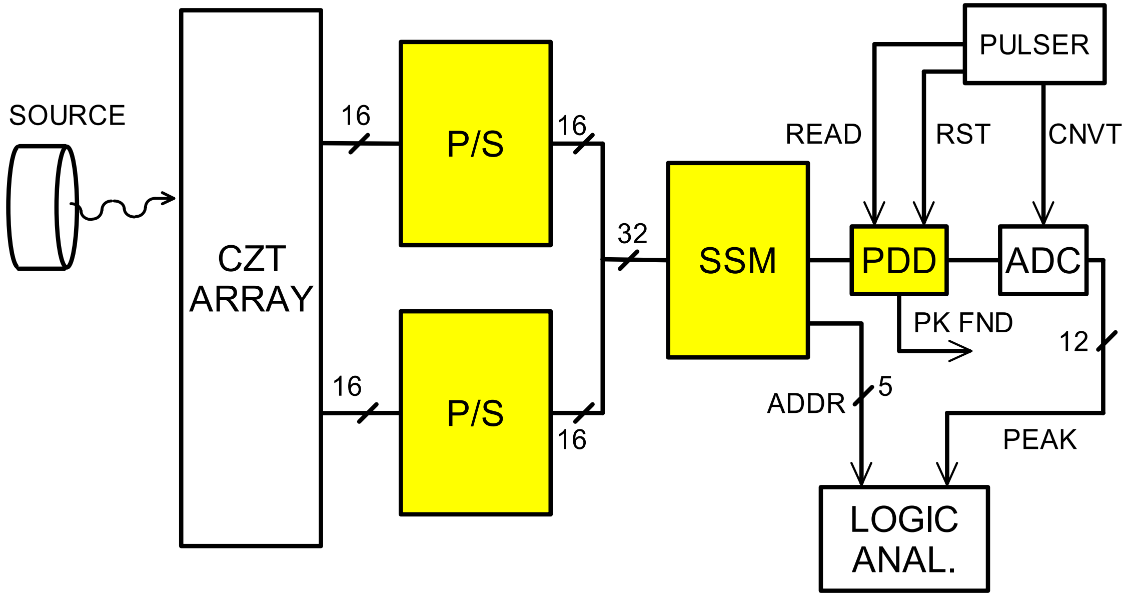
B: PD plus SCA as analog buffer



C: PD with multiple hold capacitors

Topology A with two parallel PDs has been fabricated and tested.

Multichannel Readout System with PDD

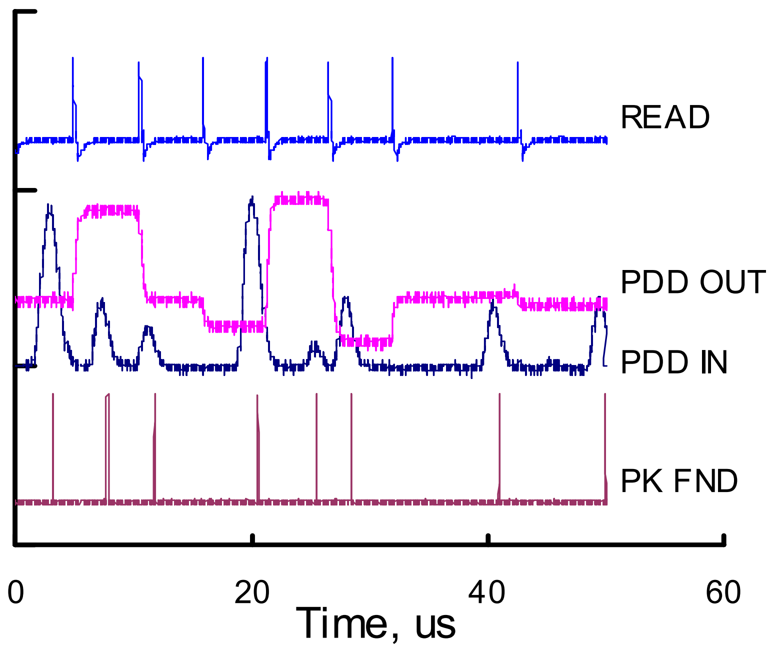


SSM: self-switched multiplexer; custom chip that detects above-threshold inputs and routes them to PDD input.

In response to a READ request from the DAQ system (pulser), the next peak sample stored in the PDD is presented to the 12-bit ADC.

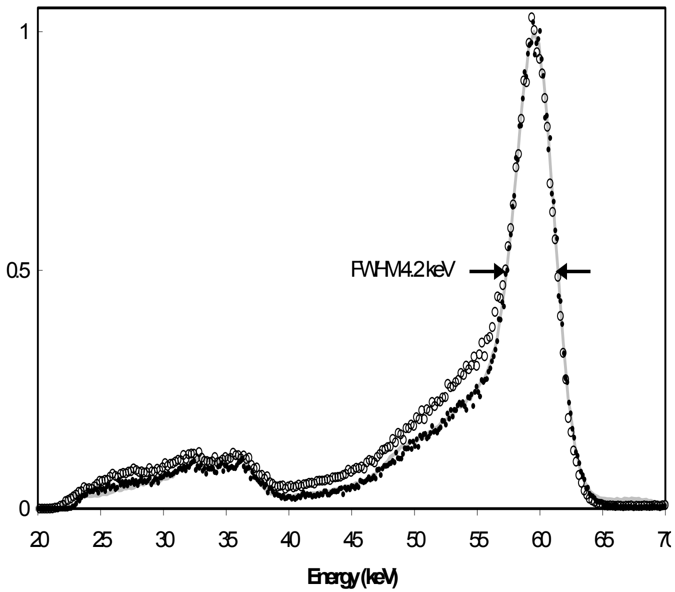
After a fixed delay the pulser RESETs the PDD that was read out, freeing it to process next input pulse.

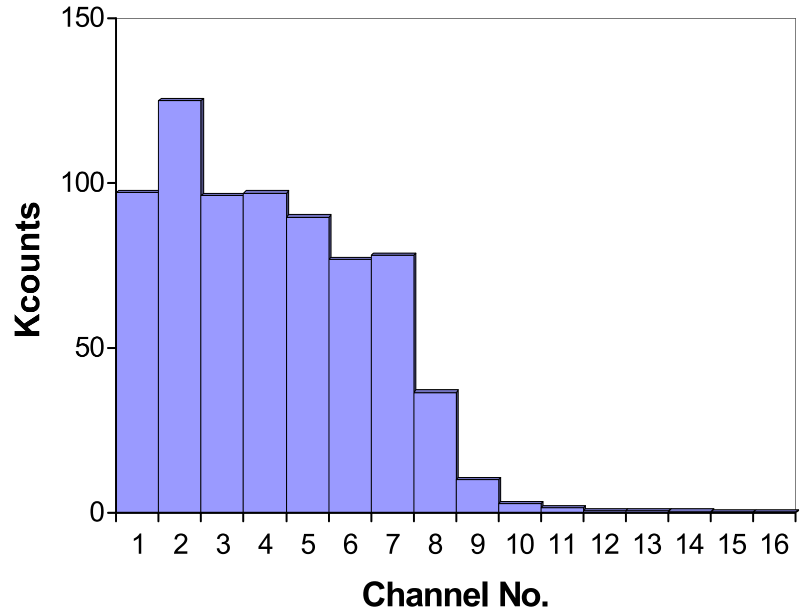
Multichannel PDD Readout System: First Results



- Input pulses from source occur randomly
- READ process is synchronous 200 kHz
- READ rate matches average input rate
- Simultaneous readout and acquisition of new data
- 2-sample buffer absorbs rate fluctuations

Multichannel PDD Readout System





<u>Spectra</u>

Solid line: commercial MCA.

Points: PDD, single channel.

Circles: PDD, 16 channels gain-adjusted.

Resolution limited by CZT detectors.

<u>Source Profile</u>

^{241}Am source centered over channel 2.

Summary

- New 2-phase peak detector in submicron CMOS:
  - *High absolute accuracy (0.2%) and linearity (0.05%)*
  - *Rail-to-rail input and output*
  - *± 2.3 ns time walk*
  - *Low power (3.5 mW)*
  - *Extremely compact (0.03 mm^2)*
- A building block for compact, efficient multichannel readout system:
  - *Self-triggered*
  - *Self-sparsifying*
  - *Deadtimeless*
- Peak detector – derandomizer (PDD) with 2-event buffer demonstrated:
  - *First step towards data-driven analog FIFO readout*